Latch-up Verification / Rule Checking Throughout Circuit Design Flow

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April 2016
Motivation

The verification of latch-up protection networks in modern integrated circuits is a difficult challenge:

- Increasing design and process complexity;
- Higher-pin counts;
- Computational difficulties in dealing with large data sets.

Traditional latch-up geometrical rule checks using DRC tools can only provide limited verification:

- Focused on layout topology;
- Electrical information for latch-up risk areas throughout the chip is not available;
- Pose a significant risk of missing hidden latch-up pitfalls.

Fully automated latch-up rule checking approach is highly desired.
Outline

- Latch-up prevention flow
- Latch-up scenarios and prevention methods
- Latch-up physical verification techniques
- Identifying and assessing risks associated with latch-up injectors
- Validating latch-up prevention techniques for the devices in grounded nwell
- Context based checking for latch-up spacing checks
- Latch-up verification case studies for guard rings and well ties
- Dual DRC and Calibre PERC-based latch-up verification flow
- Conclusions
# Latch-up Prevention Flow

## I. Identifying Latch-up Injectors

<table>
<thead>
<tr>
<th>Externally connected diffusion devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Directly connected to an I/O pad</td>
</tr>
<tr>
<td>• Connected to an I/O pad through a high current conducting path (small resistors, large switches, etc.)</td>
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</tbody>
</table>

| Diffusion devices formed in grounded Nwell or “hot” Pwell |

## II. Enabling Latch-up Prevention Design Techniques

| Surround devices that can form latching path with guard rings |
| Reduces betas and divert collector current from the base of bipolar transistors |

| Surround devices that can form latching path with well/substrate ties |
| Keeps well potential at nominal values and prevent bipolar transistors from turning on |

| Keep p and n diffusions far apart from each other |
| Increases bipolar transistor base width and lowers bipolar gain |
Latch-up Scenarios:
Pad Connected Diffusion Devices

Risk:
Current injection or supply overvoltage → PNP and NPN turn on

Cases:
- Diffusion devices directly connected to pad
- Diffusion devices connected to pad through a high current conducting path (small resistors, large switches, etc.)
Latch-up Scenarios: Grounded Nwell Devices

Risk:
Grounded Nwell, a nearby p+ in an unrelated Nwell → PNP and NPN turn on

Cases:
• Nwell directly connected to ground pad (VSS)
• Nwell connected to ground pad (VSS) through a high current conducting path (small resistors, large switches, etc.)
Latch-up Scenarios: “Hot” Pwell/Rwell Devices

Risk:
“Hot” Pwell/Rwell, a nearby n+ or Nwell at lower potential → PNP and NPN turn on

Cases:
• Pwell/Rwell directly connected to supply pad (VDD)
• Pwell/Rwell connected to supply pad (VDD) through a high current conducting path (small resistors, large switches, etc.)
Latch-up Prevention Design Techniques: Lateral Isolation

Method:
Isolation of p and n emitters with guard rings (carrier collection) and well/substrate ties (potential control)

Guard ring must have low resistance connection to supply (VDD, VSS) to provide carrier collection/potential control.
Latch-up Prevention Design Techniques: Lateral Separation

Method:
Separation (distance) of p and n emitters to weaken parasitic bipolar transistors by increasing their base width.

Required separation/distance is dependent on operating voltage:

if VDD1 > VDD2, then \( D_1(VDD1) > D_2(VDD2) \)
Latch-up Physical Verification

- Latch-up physical verification was historically based on Design Rule Checking (DRC) [T. Stultz, 1981; J. Criscuolo, 1986; L. Lavagno, 2006]
- Advanced latch-up physical verification using DRC/ERC

A flow chart to show the layout verification and modification under the development of the cell libraries [M.-D. Ker, 1997]

- Latch-up DRC [C. Robertson, 2014]:
  - 35% of ESD and latch-up rules “un-checkable” with standard EDA tools.
  - The other 65% of rules need additional manually placed marker layers.
## Latch-up DRC/ERC

<table>
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<th>Features</th>
<th>Limitations</th>
</tr>
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<tbody>
<tr>
<td>- Can verify the presence of guard rings and well/substrate ties.</td>
<td>- Cannot validate guard ring and well/substrate tie effectiveness in collecting carries – additional resistance checks are needed.</td>
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<tr>
<td>- Can validate lateral separation based on worst case (highest system voltage) scenarios.</td>
<td>- Based on worst case (highest system voltage) scenario leading to overly conservative layout. propagation of supply voltage and I/O pad voltage is needed to accurately assess latch-up risk.</td>
</tr>
<tr>
<td>- Can flag latch-up risks related to grounded Nwells and “hot” Pwells.</td>
<td>- Identification of grounded Nwells and “hot” Pwells is limited to direct connection of wells to supply. Detection of connections through current conduction devices (small resistors, forward biased diodes, transistor switches) is not possible.</td>
</tr>
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Calibre® PERC™ Latch-up Checking - Features

- Flags violations that would be missed using DRC (e.g., indirectly connected current injectors, resistive guard rings, etc.).

- Tailors latch-up checks to specific voltages used on product, allows optimizing layout area by not following conservative (highest system voltage) rules.

- Dynamically generates marker layers (limits the number of required manual marker layers).

- Provides detailed debugging information (net by layer output, net path, etc.) in addition to standard DRC output.
Identifying Latch-up Injectors using EXT Marker

Check Objective:
Ensure all diffusion devices connected to I/O pads are marked as potential latch-up aggressors/injectors.

- EXT is manually placed marker layer
- Additional latch-up separation and isolation checks are run based on identified aggressors/injectors
- Proper placement of EXT marker is validated using Calibre® PERC™

Externally connected diffusion marked with EXT layer
Identifying Latch-up Injectors using EXT Marker

Benefits:

- use of EXT marking layer provides a visual aid to the designer,
- EXT layer provides legacy compatibility between DRC and Calibre® PERC™ latch-up flows
- enables DRC based checks to be run at cell and block levels
- provides flexibility in accounting for special bonding options (e.g. test pads which are not to be bonded out) that do not require external latch-up compliance

Flowchart:

1. Find I/O Pads
2. Identify Diffusion Devices Connected To I/O Pads
3. Low Res Path
4. Device Marked With EXT Layer?
   - Yes: OK
   - No: Latch-up Error
Validating Latch-up Protection for Grounded Nwells

Check Objective:
Ensure Nwells connected to VSS do not pose latch-up risk.

- Nwell connection to VSS could be either direct or through a high current conducting path.
- Both permanent and temporary (power sequencing) connection to VSS are considered.

Find Nwell Tied to VSS

1. Yes: Unbroken, low R Pwell Guard Ring surrounds Grounded Nwell
   - Yes: Space to Non-Grounded Nwells with p+ diffusion is \( \geq D1 \)
     - Yes: OK
   - No: Latch-up Error
2. No: Space to Non-Grounded Nwells with p+ diffusion is \( \geq D1 \)
   - No: Latch-up Error

Error 2: \( D1' < D1 \)
Identifying Latch-up Guard Rings using GRING Marker

- Guard ring (GRING) marker layer helps both DRC and Calibre® PERC™ to identify intended latch-up guard rings.

- Once identified, latch-up guard ring efficiency requirements are checked:
  - Proper bias (N guard ring tied to highest potential, P guard ring to lowest potential)
  - Low resistance connection of guard ring to supply (VDD, VSS)
  - Minimum contact density
  - Minimum width
  - Exclusiveness (guard ring active area does not contain other devices which could interfere with carrier collection)
Well Tie Rule Checking

- Well ties are required to keep potential close to nominal values and, therefore, prevent parasitic bipolar transistors from turning on and forming a latch-up path.
- Well tie frequency should be higher closer to potential latch-up injectors (identified by EXT marker layer or directly through Calibre PERC)

**Layout example:**
- Core NMOS’s in Pwell with limited number of Pwell ties
- I/O PMOS in proximity to core NMOS’s, $A_1 < A_2$
- Pwell tie frequency is violated for NMOS$_1$, but not for NMOS$_2$
Indirect Connections

DRC latch-up checks cannot efficiently validate indirect electrical connections through current conduction devices (small resistors, forward biased diodes, transistor switches).

Calibre® PERC™ can detect net connectivity through current conduction devices and identify latch-up risks which would be missed with DRC.
Voltage Dependent Spacing Rule Checking

Example: Different spacing checks required based on $\Delta V$

Spacing to/from each block is different
- 5V to 5V: spacing rule 1 ($B_1$)
- 3.3V to 3.3V: spacing rule 2 ($B_2$)
- 3.3V to 5V: spacing rule 3 ($B_3$)

Complexity increases with more power domains

DRC
Differentiates spacing rules based on marker layers for different voltage nets.

Calibre® PERC™
Detects net voltage based on external pin definition file and voltage propagation method. No complex marker layers are required.
Latch-up Verification Flows

Inputs
- Latch-Up DRC Deck
- Layout
- LVS Deck
- Latch-up Calibre® PERC™ Rules

Outputs
- Calibre® RVE
- Reports
- Debug

DRC
- Partial validation of latch-up prevention techniques (limited connectivity info).
- Allows finding errors sooner in the design flow at cell and block level.

Calibre® PERC™
- Accurate validation of latch-up prevention techniques (full connectivity info).
- Requires connectivity information which may not be fully available at low levels.

Reports
- Cell Level
- Block/Macro Level
- Top Level
Rule context based checking:
- Supply voltage value
- Layout topology

Charge Pump Spacing Check Example [Oberoi, 2012]
Conclusion

There are advantages to using dual DRC/PERC flow:

- **DRC**
  - Checks are focused on layout topology with basic connectivity information and can only provide limited latch-up verification
  - Use of marker layers poses a risk of missing latch-up errors
  - Useful at early design stages when electrical information for latch-up risk areas throughout the chip is not readily available

- **Calibre® PERC™**
  - Provides fully automated latch-up rule checking by using advanced net analysis in conjunction with layout topology
  - Allows voltage aware net checking
  - Adds robustness to the latch-up flow by eliminating human errors
References


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